IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	John D. Hyde, et al.
SERIAL NO.:	10/661,037 CONFIRMATION No.: 6704
FILING DATE:	September 12, 2003
TITLE:	METHOD AND APPARATUS FOR TRIMMING HIGH-RESOLUTION DIGITAL-TO-ANALOG CONVERTER
EXAMINER:	Soward, Ida M.
ART UNIT:	2822

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date printed below:

Date: 6/10/05 Name: Sharon E. Byam

Sharon E. Byam

Mail Stop: RCE
COMMISSIONER FOR PATENTS
P.O. Box 1450
ALEXANDRIA, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Each item of information listed in the attached FORM PTO-1449, for which a copy of each is attached (unless the blanket waiver referred to below applies), may be material to the examination of the above-identified application and is, therefore, submitted in compliance with the duty of disclosure defined in 37 CFR §§ 1.56, 1.97 and 1.98. The Examiner is requested to review, consider and document each such item in the official record of this application.

Note: If this box ☒ is checked, this case was filed after June 30, 2003 and qualifies for the blanket waiver of deposit of copies of U.S. Patents and U.S. Patent Application

Publications in accordance with the written waiver of 37 CFR §1.98 (a)(2)(i) dated July 11, 2003. Accordingly, such copies are not attached.

This Information Disclosure Statement under 37 CFR §§ 1.56, 1.97 and 1.98 is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that any one or more of these items constitutes prior art.

I

This statement is filed pursuant to:

☒ **37 C.F.R. § 1.97(b).**
This information disclosure statement is filed either:
(1) within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);
(2) within three months of the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in an international application;
(3) before the mailing date of a first office action on the merits; **or**
(4) before the mailing of a first office action after the filing of a Request for Continued Examination under 37 C.F.R. §1.114, **whichever event occurs last.**

Accordingly, this information disclosure statement requires no fee and no certification.

☐ **37 C.F.R. § 1.97(c).**
This information disclosure statement is filed **after** the period specified in 37 C.F.R. § 1.97(b), but **before** the mailing date of any of the following:
(1) a final action under 37 C.F.R. § 1.113;
(2) a notice of allowance under 37 C.F.R. § 1.311; **or**
(3) an action that otherwise closes prosecution in the application.

Accordingly, this information disclosure statement requires either:
(1) the fee specified in 37 C.F.R. § 1.17(p) for submission of an information disclosure statement under 37 C.F.R. § 1.97(c); **or**
(2) a certification according to 37 C.F.R. § 1.97 (e)(1) or (2).

☐ **37 C.F.R. § 1.97(d).**
This information disclosure statement is filed **after** the period specified in 37 C.F.R. § 1.97 (c).

Accordingly, this information disclosure statement requires:
(1) a certification in accordance with 37 C.F.R. § 1.97(e); **and**
(2) the fee specified in 37 C.F.R. § 1.17 (p) to consider an information disclosure statement under 37 C.F.R. § 1.97(d).

If this statement crosses in the mail with an office action, or is otherwise not in the indicated category of 37 C.F.R. § 1.97, it is respectfully requested that this statement be treated in the next appropriate category and made of record. **To the extent required, please treat this paper as a conditional petition for acceptance of the information disclosure statement.**

II

Fees Due:

☒ No fee is due.

☐ The fee specified in 37 C.F.R. § 1.17(p) for submission of an information disclosure statement under 37 C.F.R. § 1.97(c) or 37 C.F.R. § 1.97(d) is enclosed (**$180**).

III

Certification:

☒ No certification is necessary.

☐ Pursuant to 37 C.F.R. § 1.97(e)(1), the undersigned hereby certifies:
That each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

☐ Pursuant to 37 C.F.R. § 1.97(e)(2), the undersigned hereby certifies:
No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

IV

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please charge any additional required fee or credit any overpayment to our deposit account number 50-1698.

Respectfully submitted,
THELEN REID & PRIEST LLP

Dated: 6/10/'05

Khaled Shami
Reg. No. 38,745

THELEN REID & PRIEST LLP
P.O. Box 640640
San Jose, CA 95164-0640
(408) 292-5800 direct dial
(408) 287-8040 direct fax

Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0003D1	Serial No.: 10/661,037
Information Disclosure Statement by Applicant	Applicant: John D. Hyde et al.	
(Use several sheets if necessary)	Filed: September 12, 2003 Group: 2822	

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
	A	2003/0206437	11/6/2003	Diorio et al.			
	B	2004/0004861	1/5/2004	Srinivas et al.			
	C	2004/0021166	2/5/2004	Hyde et al.			
	D	2004/0037127	2/26/2004	Lindhorst et al.			
	E	2004/0052113	3/18/2004	Diorio et al.			
	F	5,627,392	5/6/1997	Diorio et al.			
	G	5,633,518	5/27/1997	Broze			
	H	5,666,118	9/9/1997	Gersbach			
	I	5,666,307	9/9/1997	Chang			
	J	5,687,118	11/11/1997	Chang			
	K	5,691,939	11/25/1997	Chang et al.			
	L	5,706,227	1/6/1998	Chang et al.			
	M	5,736,764	4/7/1998	Chang			
	N	5,841,165	11/24/1998	Chang et al.			
	O	5,875,126	2/23/1999	Minch et al.			

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No
	P	0 776 049	5/28/1997	EP			X	
	Q	0 778 623	07/18/2001	EP			X	

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

	R	Chang, et al., "A CMOS-Compatible Single-Poly Cell for Use as Non- Volatile Memory", International Semiconductor Device Date Research Symposium, December 1-3, 1999.
	S	Chang, et al., "Non-Volatile Memory Device with True CMOS Compatibility", Electronics Letters, Vol. 35, No. 17, August 19, 1999, pp. 1443- 1445.
	T	Chung, et al., "N-Channel Versus P- Channel Flash EEPROM-Which One Has Better Reliabilities", IEEE Annual International Reliability, 2001, pp. 67-72.
	U	Declercq, et al., "Design and Optimization of High-Voltage CMOS Devices Compatible with a Standard 5 V CMOS Technology", IEEE Custom Integrated Circuits Conference, 1993, pp. 24.6.1-24.6.4
	V	Diorio, et al., "Adaptive CMOS: From Biological Inspiration to Systems-on-a-Chip"; IEEE, Vol 90, No. 3; March 2002; pp 345-357.
	W	Diorio, et al., "A Floating-Gate MOS Learning Array with Locally Computed Weight Updates" IEEE Transactions on Electron Devices, vol. 44, No. 12, December 1997, pp. 1-10.

Examiner	Date Considered

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0003D1	Serial No.: 10/661,037
Information Disclosure Statement by Applicant	Applicant: John D. Hyde et al.	
(Use several sheets if necessary)	Filed: September 12, 2003	Group: 2822

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
	X	5,898,613	4/27/1999	Diorio et al.			
	Y	5,912,842	6/15/1999	Chang et al.			
	Z	5,914,894	6/22/1999	Diorio et al.			
	AA	5,966,329	10/12/1999	Hsu et al.			
	AB	5,986,927	11/16/1999	Minch et al.			
	AC	5,990,512	11/23/1999	Diorio et al.			
	AD	6,055,185	4/25/2000	Kalnitsky et al.			
	AE	6,081,451	6/27/2000	Kalnitsky et al.			
	AF	6,125,053	9/26/2000	Diorio et al.			
	AG	6,137,723	10/24/2000	Bergemont et al.			
	AH	6,137,724	10/24/2000	Kalnitsky et al.			
	AI	6,144,581	11/7/2000	Diorio et al.			
	AJ	6,166,954	12/26/2000	Chern			
	AK	6,190,968	2/20/2001	Kalnitsky et al.			
	AL	6,208,557	3/27/2001	Bergemont et al.			

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	Diorio, et al., "A High-Resolution Non-Volatile Analog Memory Cell", IEEE, 1995, pp. 2233-2236.
	AN	Diorio, "A p-Channel MOS Synapse Transistor with Self-Convergent Memory Writes", IEEE Transaction On Electron Devices, Vol. 47, No. 2, pp. 464-472, February 2000.
	AO	Hasler, et al., "An Autozeroing Amplifier Using PFET Hot-Electron Injection", IEEE, 1996.
	AP	Hasler, et al., "Single Transistor Learning Synapses", Cambridge, MA, The MIT Press, 1995, pp. 817-824.
	AQ	Hasler, et al., "Single Transistor Learning Synapse with Long Term Storage", IEEE, 1995, pp. 1660-1663.
	AR	Hasler, et al., "An autozeroing Floating-Gate Amplifier", IEEE Transactions on Circuits and Systems, Analog and Digital Signal Processing, Vol. 48, No. 1, January 2001, pp. 74-82.

Examiner	Date Considered

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0003D1	Serial No.: 10/661,037
Information Disclosure Statement by Applicant	Applicant: John D. Hyde et al.	
(Use several sheets if necessary)	Filed: September 12, 2003 Group: 2822	

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
	AS	6,222,771	4/24/2001	Tang et al.			
	AT	6,452,835	9/17/2002	Diorio et al.			
	AU	6,479,863	11/12/2002	Caywood			
	AV	6,534,816	5/18/2003	Caywood			

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	Hyde, et al.; "A Floating-Gate Trimmed, 14-Bit, 250 Ms/s Digital-to-Analog Converter in Standard 0.25 um CMOS", Impinj, 2002 Symposium on VLSI Circuits, Honolulu HI; pp 328-331.

Examiner	Date Considered

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.